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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/727,887	12/04/2003	Paul Rudeck	400.180US03	6757

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EXAMINER	
THOMAS, TONIAE M	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 11/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/727,887	RUDECK, PAUL	
	Examiner	Art Unit	
	Toniae M. Thomas	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/04/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is a first Office action on the merits of Application Serial No. 10/727,887, filed on 04 December 2004, which is a continuation of Application Serial No. 10/224,915, filed on 21 August 2002, now US Patent 6,762,093.

2. Currently, claims 1-17 are pending.

Specification

3. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 3-8, and 10 are rejected under 35 U.S.C. 103(a) as being obvious over Cloud et al. (US 6,297,989 B1) in view of Kao (US 6,323,514 B1).[1]

The applied references US 6,297,989 B1 (Cloud et al.) and Kao (US 6,323,514 B1) have a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art

[1] Applicant submitted the Cloud et al. patent as prior art.

only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). For applications filed on or after November 29, 1999, this rejection might also be overcome by showing that the subject matter of the reference and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person. See MPEP § 706.02(l)(1) and § 706.02(l)(2).

The Cloud et al. patent (Cloud) discloses a method of forming a floating gate transistor (fig. 2 and col. 4, line 52 - col. 5, line 30). The method comprises the steps of: forming laterally spaced source and drain regions 215, 216 to define a channel 214 there between (fig. 2 and col. 4, lines 65-66); forming a substantially flat floating gate portion 212 above the channel region (fig. 2; col. 4, lines 61-64; and col. 5, lines 11-15); forming a contact 230 coupled to the flat floating gate portion at an exposed region, the contact

extending vertically above the flat floating gate portion (fig. 2 and col. 5, lines 11-14); forming a vertically extending floating gate container portion 221 coupled to the contact, the floating gate container portion having interior and exterior regions (fig. 2 and col. 5, lines 11-15); and forming a control gate 223 adjacent to the floating gate container portion (fig. 2 and col. 5, lines 15-28).

Cloud lacks anticipation in not teaching the steps of: forming spacers over the flat floating gate portion to define an exposed region on the flat floating gate portion; and forming the floating gate container portion from a hemispherical grain (HSG) polysilicon material. However, Kao discloses a method for forming a floating gate (figs. 1-6 and accompanying text). The method comprises forming spacers 20 over a first floating gate portion 14 (fig. 2 and col. 3, lines 5-9), and forming a polysilicon vertically extending container 50 comprising an HSG material (fig. 6; col. 3, lines 66 - col. 4, line 12; and col. 4, lines 33-36).

Since the Cloud and Kao patents are from the same field of endeavor, the purpose for which Kao is relied upon would have been recognized in the pertinent reference of Cloud by one of ordinary skill in the art at the time the invention was made.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify Cloud in view of Kao, by forming spacers over the floating gate portion 212 and forming the container 221 comprising HSG, as taught by Kao, for the following reasons: forming spacers over the

floating gate portion prohibits the sidewalls of the floating gate portion from being damaged during subsequent processing steps; and forming the container 221 such that it comprises an HSG material increases the coupling coefficient between the floating gate and control gate (Kao -col. 2, lines 2-8).

5. *Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cloud in view of Kao as applied to claim 1 above, and further in view of Liu et al. (US 6,329,277 B1).*

As discussed above, Kao discloses a method of forming a floating gate transistor, wherein the method comprises forming spacers over a flat floating gate portion. While Kao discloses forming spacers over a flat floating gate portion, Kao does not teach that the spacers are nitride spacers, as recited in claim 3. The spacers are oxide spacers (Kao - col. 3, lines 33-36). However, the Liu et al. patent (Liu) discloses a method for forming a floating gate transistor (figs. 7-9 and accompanying text). The method comprises forming spacers 25 over a flat floating gate portion 21 (col. 5, lines 46-48 and lines 56-58). The spacers are formed from either a silicon dioxide material or a silicon nitride material (col. 5, lines 56-58). Liu suggests that silicon dioxide and silicon nitride are art-recognized equivalent materials used to form sidewall spacers in floating gate transistors.

Since Kao and Liu are from the same field of endeavor, the purpose for which Liu is relied upon would have been recognized in the pertinent reference of Kao by one of ordinary skill in the art at the time the invention was made.

As discussed above, Kao teaches forming oxide spacers over a floating gate portion. It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the combination of Cloud and Kao in view of Liu by replacing the oxide spacers with nitride spacers, as taught by Liu, since silicon dioxide and silicon nitride are art-recognized equivalent materials used to form sidewall spacers in floating gate transistors.

6. *Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cloud in view of Kao as applied to claim 5 above, and further in view of Chi (US 5,981,335).* [2]

While Cloud discloses forming the flat floating gate portion from a polysilicon material (Cloud - col. 4, lines 61-62), Cloud lacks anticipation in not teaching that the contact 230, the container 221, and the control gate 223 are formed from a polysilicon material.

Chi discloses a method for forming a floating gate transistor (figs. 3b, 3c, and col. 5, line 21 - col. 6, line 5). The method comprises forming a first floating gate portion 230 laterally extending over a tunnel oxide 225 and positioned above a channel 260 (fig. 3c and col. 5, line 47 - col. 6, line 5); forming a contact 230 over the first floating gate portion, such that the contact is coupled to the first floating gate portion (fig. 3c and col. 5, line 47 - col. 6, line 5); forming a second floating gate portion 240 vertically extending above the contact, such that the second floating gate portion is coupled to the contact

(fig. 3c and col. 5, line 47 - col. 6, line 5); depositing a dielectric layer 245 over the second floating gate portion (fig. 3c and col. 5, line 47 - col. 6, line 5); and forming a control gate 250 over the dielectric layer (fig. 3c and col. 5, line 47 - col. 6, line 5). The first floating gate portion, the contact, the second floating gate portion, and the control gate are all formed from polysilicon (col. 5, line 47 - col. 6, line 5).

Since Cloud and Chi are from the same field of endeavor, the purpose for which Chi is relied upon would have been recognized in the pertinent reference of Cloud by one of ordinary skill in the art at the time the invention was made.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the combination of Cloud and Kao, by forming the contact 230, the container 221, and the control gate 223 from a polysilicon material, as taught by Chi, since polysilicon (i.e. doped polysilicon) is a highly conductive material often used to form gate electrodes in transistors.

Claims 11-14, 16, and 17 are rejected under 35 U.S.C. 103(a) as being obvious over Cloud in view of Chi and Kao.

As stated above, the applied references US 6,297,989 B1 (Cloud) and Kao (US 6,323,514 B1) have a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be

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[2] Applicant submitted the Chi patent as prior art.

overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). For applications filed on or after November 29, 1999, this rejection might also be overcome by showing that the subject matter of the reference and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person. See MPEP § 706.02(l)(1) and § 706.02(l)(2).

Cloud discloses a method of forming a floating gate transistor (fig. 2 and col. 4, line 52 - col. 5, line 30). The method comprises the steps of: forming laterally spaced source and drain regions 215, 216 into a substrate 211 to define a channel 214 there between (fig. 2 and col. 4, lines 65-66); growing a layer of tunnel oxide 213 over the substrate (col. 4, lines 59-61); depositing a polysilicon first floating gate portion 212 laterally extending over the tunnel oxide and positioned above the channel (fig. 2; col. 4, lines 61-64; and col. 5, lines 11-15); forming a contact 230 over the first floating gate portion, such

that the contact is coupled to the first floating gate portion (fig. 2 and col. 5, lines 11-14); forming a vertically extending container 221 above the contact, such that the container is coupled to the contact (fig. 2 and col. 5, lines 11-15); depositing a layer of oxide over the container (fig. 2 and col. 5, lines 20-30); and forming a control gate over the layer of oxide, wherein the control gate vertically descends into a central opening of the container (fig. 2 and col. 5, lines 15-28).

Cloud lacks anticipation in not teaching the following limitations: forming spacers over the first floating gate portion 212 forming the contact 230, the container 221, and the control gate from polysilicon; and forming the container 221 comprising HSG.

Chi discloses a method for forming a floating gate transistor (figs. 3b, 3c, and col. 5, line 21 - col. 6, line 5). The method comprises forming a first floating gate portion 230 laterally extending over a tunnel oxide 225 and positioned above a channel 260 (fig. 3c and col. 5, line 47 - col. 6, line 5); forming a contact 230 over the first floating gate portion, such that the contact is coupled to the first floating gate portion (fig. 3c and col. 5, line 47 - col. 6, line 5); forming a second floating gate portion 240 vertically extending above the contact, such that the second floating gate portion is coupled to the contact (fig. 3c and col. 5, line 47 - col. 6, line 5); depositing a dielectric layer 245 over the second floating gate portion (fig. 3c and col. 5, line 47 - col. 6, line 5); and forming a control gate 250 over the dielectric layer (fig. 3c and col. 5, line 47 - col. 6, line 5). The first floating gate portion, the contact, the second floating

gate portion, and the control gate are all formed from polysilicon (col. 5, line 47 - col. 6, line 5).

Kao discloses a method for forming a floating gate (figs. 1-6 and accompanying text). The method comprises forming spacers 20 over a first floating gate portion 14 (fig. 2 and col. 3, lines 5-9), and forming a polysilicon vertically extending container 50 comprising an HSG material (fig. 6; col. 3, lines 66 - col. 4, line 12; and col. 4, lines 33-36).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify Cloud in view of Chi by forming the contact 230, the container 221, and the control gate 223 from a polysilicon material, as taught by Chi, since polysilicon (i.e. doped polysilicon) is a highly conductive material often used to form gate electrodes in transistors. It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify Cloud in view of Kao, by forming spacers over the first floating gate portion 212 and forming the container 221 comprising HSG, as taught by Kao because: forming spacers over the floating gate portion prohibits the sidewalls of the floating gate portion from being damaged during subsequent processing steps; and forming the container such that it comprises an HSG material increases the surface area of the container and, thereby increases the coupling coefficient between the floating gate and control gate (Kao -col. 2, lines 2-8)

7. *Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cloud in view of Chi and Kao as applied to claim11 above, and further in view of Liu.*

As discussed above, Kao discloses a method of forming a floating gate transistor, wherein the method comprises forming spacers over a flat floating gate portion. While Kao discloses forming spacers over a flat floating gate portion, Kao does not teach that the spacers are nitride spacers, as recited in claim 3. The spacers are oxide spacers (Kao - col. 3, lines 33-36). However, Liu discloses a method for forming a floating gate transistor (figs. 7-9 and accompanying text). The method comprises forming spacers 25 over a flat floating gate portion 21 (col. 5, lines 46-48 and lines 56-58). The spacers are formed from either a silicon dioxide material or a silicon nitride material (col. 5, lines 56-58). Liu suggests that silicon dioxide and silicon nitride are art-recognized equivalent materials used to form sidewall spacers in floating gate transistors.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the combination of Cloud, Chi, and Kao in view of Liu by replacing the oxide spacers with nitride spacers, as taught by Liu, since silicon dioxide and silicon nitride are art-recognized equivalent materials used to form sidewall spacers in floating gate transistors.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toniae M. Thomas whose telephone number is (571) 272-1846. The examiner can normally be reached on Monday-Thursday from 8:30 a.m. to 5:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TMT
31 October 2004

Mary Wilczewski
Primary Examiner